REMARKS

The Examiner's allowance of claims 7 and 8 is acknowledged and appreciated.

Claims 5 and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. (U.S. 6,603,453) in view of Yamazaki et al. (US 2001/0052950 A1) and Nakajima et al. (5,585,647). Applicants respectfully traverse this rejection because the cited references, even if combined, still would not disclose or suggest at least the second gate insulation film being formed on, and in direct contact with, the first gate insulation film. A first gate electrode is formed on the second gate insulation films.

The present invention includes a first thin film transistor (TFT) and a second thin film transistor (TFT). The first TFT includes a first gate electrode formed on a second gate insulation film, which is formed on, and in direct contact with, the first gate insulation film. The second TFT includes a second gate electrode which is formed between the first gate insulation film and the second gate insulation film. The first and second gate insulation films are the same in both the first and second TFTs.

The Examiner asserts that the Yamazaki et al. '453 reference discloses "a first gate insulation film 805, a second gate insulation film 808, gate electrode 813 on the second gate insulation film." Figs. 1 and 16 of Yamazaki et al. '453 show a first gate insulation film (105, 805) formed on an underlying film (102, 802), and a semiconductor active layer (106, 806) provided directly over the first gate insulation film (105, 805). The second gate insulation film (108, 808) is then provided directly over the active layer (106, 806), and a gate electrode (113, 813) provided on the second gate insulation film (108, 808).

In the present invention, the first TFT includes a second gate insulation film which is formed on, and in direct contact with, the first gate insulation film. A first gate electrode is formed on the second gate insulation film. In contrast, the Yamazaki et al. '453 reference clear teaches that the second gate insulation film (108, 808) is formed on top of the semiconductor active layer (106, 806), which is formed on the first gate insulation film (105, 805). In other words, Yamazaki et al. '453 teaches inserting the semiconductor active layer between the second and the first gate insulation films. Therefore, the Yamazaki et al. '453 reference cannot disclose a second gate insulation film which is formed on, and in direct contact with, the first gate insulation film, as described in claim 5.

The Yamazaki et al. '950 reference is cited merely for disclosing a gate insulation layer being formed over a semiconductor layer and having a lightly doped region. This reference also does not disclose or suggest the second gate insulation film being formed on, and in direct contact with, first gate insulation film, as in the present invention.

The Nakajima et al. reference is cited for disclosing, in Fig. 8C, both first and second gate electrodes 44b and 44a being "located between first insulating film 43 and a second insulating film 45" (emphasis added). Clearly, this reference cannot disclose the second gate electrode being provided on the second gate insulation film.

As described above, none of the cited references, alone or in combination teaches or suggests the second gate insulation film being formed on, and in direct contact with, the first gate insulation film, and the first gate electrode being formed on the second gate insulation film. Claims 5 and 6 are allowable for at least this reason.

Applicants now believe the application is in condition for allowance, which is respectfully requested. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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